AMENDMENTS TO THE SPECIFICATION

Please amend the second complete paragraph on page 3 of the specification with the following replacement paragraph:

One technique for adjusting the critical timing edges of macros within an integrated circuit is the use of self-timed pulse control (STPC) circuits to change the timing of supplied clock signals. An exemplary STPC system is described in U.S. Patent No. 5,964,884 [[5,964,844]], entitled, "Self-timed pulse control circuit," and incorporated herein by reference in its entirety. In general an STCP circuit provides a variable amount of delay in the path traversed by the clock signal that is supplied to a macro. In one example, six alternate clock paths may be provided, with each path having a varying delay characteristic. The specific number of paths depend on the particular macro and the granularity of the control desired.

Please amend the paragraph beginning at line 9 on page 14 with the following replacement paragraph:

Referring briefly to Figure 4, a graph 400 illustrating performance data gathered through the method of Figure 3 is provided. The timing sensitivity for Macro 1 (*i.e.*, operating voltage of 2.0 volts) is shown by a curve 410, and the timing sensitivity for Macro 2 (*i.e.*, operating voltage of 2.0 volts) is shown by a curve 420. The curve 410 demonstrates that Macro 1 has little contribution to the critical timing path of the device under test 120. However, the curve 420 illustrates that Macro 2 has a significant effect on the critical timing path of the device under test 120. As discussed above with reference to Figure 3, the vertical axis of the graph 400 indicates a maximum frequency and the horizontal axis indicates an STPC offset.